REMARKS

Claims 1-3 are pending. Reconsideration and allowance in view of the following remarks are respectfully amended.

Claims 1-3 were rejected under 35 U.S.C. § 102(b) over Hsu (U.S. Patent 4,764,482). The rejection is respectfully traversed.

Claim 1 recites, *inter alia*, forming a first type well with shallow junction in peripheral regions of the second device isolation structure and a region between the first device isolation structure and the second device isolation structure.

The Examiner alleges on page 3, lines 10-12, of the Office Action that the source region 40 of Hsu corresponds to this claimed feature. However, the source region 40 is formed in the P-type region 14 by arsenic implantation. It is not formed in the peripheral regions of a second device isolation structure (which is a structure with a trench, as discussed in more detail below), nor in a region between a first device isolation structure (which is formed by partial oxidation, as discussed in more detail below). Accordingly, Hsu doe not anticipate claim 1.

Claim 1 also recites, *inter alia*, forming a second type well with shallow junction in peripheral regions of the first device isolation structure and a region of the second device isolation structure.

The Examiner alleges on page 3, lines 13-14, of the Office Action that the P-type pocket regions 30 of Hsu corresponds to this claimed feature. However, the P-type pocket regions 30 are formed by implantation in the area where the PMOS device will be located. They are not formed in the peripheral regions of a first device isolation structure and a region of a second device isolation structure (which is formed by partial oxidation, as discussed in more detail below). Therefore, Hsu doe not anticipate claim 1.

Claim 1 further recites, *inter alia*, forming a first device isolation region through partial oxidation in the first area and forming a second device isolation region with a trench in a second area of the semiconductor substrate.

Hsu discloses that the silicon dioxide isolation regions 18 are formed by conventional local oxidation of silicon (LOCOS) techniques, or a trench isolation region (not shown) could be used in place of the regions 18 formed by the LOCOS technique. Hsu does not disclose a first device isolation region formed through partial oxidation in the first area and a second device isolation region formed with a trench in a second area of the semiconductor substrate. Hsu, thus, cannot anticipate claim 1.

Claims 2 and 3 recite additional features of the invention and are allowable for the same reasons discussed above with respect to claim 1 and for the additional features recited therein.

Reconsideration and withdrawal of the rejection of claims 1-3 over Hsu are respectfully requested.

In view of the above amendments and remarks, Applicants respectfully submit that the all the claims are allowable and that the entire application is in condition for allowance.

Should the Examiner believe that anything further is desirable to place the application in better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,
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